

INTEGRATED CIRCUIT DEVICES HAVING HIGH PRECISION DIGITAL DELAY LINES THEREIN

Abstract of the Disclosure

Integrated circuit delay devices include a digital delay line that is configured to provide a percent-of-clock period delay to a timing signal accepted at an enabled one of a plurality of injection ports thereof. The digital delay line may be responsive to an injection control signal having a value that sets a length of the delay by specifying a location of the enabled one of the plurality of injection ports, with the end of the delay line being a fixed output port. A delay line control circuit is also provided that is responsive to a clock signal having a period from which the percent-of-clock period delay is preferably measured. The delay line control circuit is configured to generate the injection control signal by counting multiple cycles of a high frequency ring oscillator signal having a period less than, and typically substantially less than, the clock period, over a time interval having a duration greater than, and typically substantially greater than, the clock period. The ring oscillator signal may be generated by a ring oscillator having a relatively small number of stages and the time interval may be sufficiently long so that a large number of cycles of the ring oscillator signal may be counted over many periods of the clock signal.

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